UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/812,147 | 03/29/2004 | Louis B. Hobson | 200314997-1 | 2982 |

22879 7590 04/12/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

| EXAMINER | |
|---|---|
| PLANTE, JONATHAN R | |
| ART UNIT | PAPER NUMBER |
| 2182 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 04/12/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/812,147 | HOBSON, LOUIS B. | |
| | Examiner | Art Unit | |
| | Jonathan R. Plante | 2182 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is in response to the applicant's communication filed 06 February 2007 in response to PTO Office Action mailed 06 November 2006 for Application 10/812,147. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-24 have been presented for examination in this application. As a result, claims 1-24 are now pending in this application. Claims 1, 11, 14, 22, 23, and 24 are independent claims.

### *Claim Amendments*

3. Acknowledgment of receiving amendments to the claims, which were received by the Office on 06 February 2007. Claims 1, 9, 10, 11, and 12 are amended.

The following objections are withdrawn based on Applicants alternative detailed in amendment filed on 06 February 2007:

a. (Claim 1, Line 5): Examiner agrees to the change of "**may be**" to "are selectively".

b. (Claim 1, Line 7): Examiner agrees to the change of "**that can be**" to "that is selectively".

c. (Claim 12, Line 5): Examiner agrees to the change of "**may be**" to "are selectively".

d. (Claim 12, Line 7): Examiner agrees to the change of "**that can be**" to "that is selectively".

All other objections are withdrawn due to the amendment and remarks filed on 06 February 2007.

***Drawing Amendments***

4. Applicant is informed that the Office DID NOT receive amended drawings as indicated "**the drawing sheets have been amended as requested**" (Amendment A, Page 14).

However, the objections to the drawings per Office Action mailed 06 November 2006 have been withdrawn due to amendments and remarks filed 06 February 2007.

***Specification Amendments***

5. Acknowledgement of receiving amendments to the specification, which were received by the Office on 06 February 2007.

The objections to the specification per Office Action mailed 06 November 2006 have been withdrawn due to amendments and remarks filed 06 February 2007.

***Specification Objections***

6. The use of the trademarks:
    a. (Paragraph 0024): Pentium
    b. (Paragraph 0048): Infiniband
    c. (Paragraph 0049): Bluetooth
    d. (Paragraph 0053): Java

have been noted in this application. Applicant should capitalize each letter of the trademark/copyright or include the proper trademark symbol, such as ™ or ® following the word and be accompanied by the generic terminology. (MPEP 608.01(v))

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

***Claim Amendments***

7. Acknowledgement of receiving amendments to the claims, which were received by the Office on 06 February 2007.

The objections to the claims per Office Action mailed 06 November 2006 have been withdrawn due to amendments and remarks filed 06 February 2007.

***Claim Objections***

8. Claims 4, 12, 14, 16, 22, 23, and 24 are objected to because of the following informalities:
    a. (Claim 4, Line 2): Please replace "**stored in a memory**" with "stored in the memory" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.
    b. (Claim 12, Line 6): Please replace "**a thermal management signal**" with "the simulated thermal management signal" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.
    c. (Claim 14, Line 3): Please replace "**a processor performance state**" with "the processor performance state" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.
    d. (Claim 14, Line 6): Please replace "**controlling the state**" with "controlling a state" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.
    e. (Claim 15, Line 2): Please replace "**ACPI table in**" with "ACPI table store in" to resolve a potential 35 U.S.C. 101 rejection.
    f. (Claim 16, Line 2): Please replace "**the address of the**" with "a address of the" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.
    g. (Claim 22, Line 1): Please replace "**computer-readable medium**" with "computer-readable storage medium" to resolve 35 U.S.C. 101 rejections. Please see 35 U.S.C. 101 rejections.

h. (Claim 22, Line 4): Please replace "**a processor performance state**" with "the processor performance state" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.

i. (Claim 22, Line 4): Please replace "**a processor**" with "the processor" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.

j. (Claim 22, Line 7): Please replace "**controlling the state**" with "controlling a state" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.

k. (Claim 22, Line 10): Please replace "**to a thermal management signal**" with "to the thermal management signal" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.

l. (Claim 23, Line 8): Please replace "**simulating a processor performance**" with "simulating the processor performance" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.

m. (Claim 24, Line 2): Please replace "**computer-readable medium**" with "computer-readable storage medium" to resolve 35 U.S.C. 101 rejections. Please see 35 U.S.C. 101 rejections.

n. (Claim 24, Line 7): Please replace "**related to a simulated processor**" with "related to the simulated processor" to resolve potential lack of antecedent basis issues and for claim clarity and completeness.

Appropriate correction is required.

***Claim Amendments 35 USC § 112***

9. The 35 U.S.C. § 112 first paragraph and second paragraph rejections to the claims per Office Action mailed 06 November 2006 have been withdrawn due to amendments and remarks filed 06 February 2007.

***Claim Rejections - 35 USC § 112***

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

    The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 7, 8, 13, 19, and 20 are rejected under 35 U.S.C. 112, second paragraph, for the presence of trademarks or trade names in the claims. Please see **MPEP 2173.05(u) "Trademarks or Trade Names in a Claim"**.

    a. (Claim 7, Line 2) is rejected for the presence of "**TM2 register**" and "**Pentium microprocessor**". The Examiner will evaluate these terms using generic term equivalents of "a thermal management register" and "a microprocessor".

    b. (Claim 8, Line 2) is rejected for the presence of "**PROCHOT**" and "**Pentium microprocessor**". The Examiner will evaluate these terms using generic term equivalents of "a control line" and "a microprocessor".

    c. (Claim 13, Line 1) is rejected for the presence of "**a Pentium 4 microprocessor**". The Examiner will evaluate this term using generic term equivalent of "a microprocessor".

    d. (Claim 19, Line 2) is rejected for the presence of "**TM2 register**" and "**Pentium microprocessor**". The Examiner will evaluate these terms using generic term equivalents of "a thermal management register" and "a microprocessor".

    e. (Claim 20, Line 2) is rejected for the presence of "**PROCHOT**" and "**Pentium microprocessor**". The Examiner will evaluate these terms using generic term equivalents of "a control line" and "a microprocessor".

12. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(Claim 11) Applicant claims that "a processor that is configured to receive an actual thermal management signal from a thermal management circuit" (Claim 11, Line 1), but then claims "a combination logic configured to selectively provide to the processor one and only one of, the actual thermal management signal and the simulated thermal management signal" (Claim 11, Line 8) this leads to being indefinite in respect to the "actual thermal management signal". In one case the "actual thermal management signal" is directly provided to the processor while in the second case another signal from the "combination logic" can indirectly provide either the "actual thermal management signal" or the "simulated thermal management signal". This leads to being indefinite for the "combinational logic" is not directly providing the "actual thermal management signal", the "combinational logic" is providing another separate signal based on the logic of the circuit to the processor. It is also noted that the "actual thermal management signal" is provided to the process in two ways the first directly and as claimed affecting the "operating frequency" and a second indirect means (combination logic) that has no corresponding affect.

The Examiner additionally refers to Applicant's discloser "Figure 3" that clearly discloses that the "actual thermal management signal" and the "simulated thermal management signal" are separate inputs to the "Combination Logic" and then outputted to the processor as a distinct signal, the "PROCHOT" signal.

The Examiner recommends the following changes to Claim 11 to resolve the indefinite issues and to correspond to the written description and Figure 3:

"A system for simulating a processor performance state in a processor that is configured to receive a ~~an actual~~ thermal management signal from a combination logic ~~thermal management circuit~~ and to selectively change the processor operating frequency based on the ~~actual~~ thermal management signal, the system comprising:

a simulation logic configured to produce a simulated thermal management signal; ~~and~~

a thermal management circuit configured to produce an actual thermal management signal; and

the a combination logic configured to selectively provide to the processor one and only one of, the actual thermal management signal and the simulated thermal management signal."

Please see attachment for clean copy of suggested replacement.

***Claim Amendments 35 USC § 101***

13. The 35 USC § 101 rejections to claims 1-10, and 12-13 per Office Action mailed 06 November 2006 have been withdrawn due to amendments and remarks filed 06 February 2007.

***Claim Rejections - 35 USC § 101***

14. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 11, 23 are rejected as a result of the Applicants disclosure pertaining to the provided definition of "Logic" (Page 3, Line 29) the application defines "logic" as:

> Includes but is not limited to hardware, firmware, software and /or combinations of each to perform a function(s) or an action(s), and/or to cause a function or action from another logic, method, and/or system. For example, based on a desired application or needs, logic may include a software controlled microprocessor, discrete logic like an application specific integrated circuit (ASIC), a programmed logic device, a memory device containing instructions, or the like. Logic may include one or more gates, combinations of gates, or other circuit components. Logic may also be fully embodied as software.

As a result of "logic" being defined by Applicant in the written description as being capable of being "fully embodied as software" Claim 11 is rejected as being "functional descriptive material" (MPEP 2106.01 [R5]) since both the "simulation logic" (Claim 11, Line 6) and the "combination logic" (Claim 11, Line 8) as disclosed by applicant can be "fully embodied as software".

(Claim 11), in order to vacate this rejection the Applicant is requested to either remove "Logic may also be fully embodied as software." (Page 4, Line 4) from the written description or amend Claim 11 so that the "simulation logic" and "combination logic" become statutory by becoming structurally and functionally interrelated to a computer-readable medium (**MPEP 2106.01 [R5]**).

(Claim 23), in order to vacate this rejection the Applicant is requested to remove "Logic may also be fully embodied as software." (Page 4, Line 4) from the written description since Claim 23 is a "means for" claim, and in response to this Office action the Applicant is requested to acknowledge that the above is withdrawn from the Application for the record.

Claims 22 and 24 are rejected as a result of the applications disclosure pertaining to the provided definition of a "computer-readable medium" (Page 3, Line 9-24) the application defines a "computer-readable medium" as:

> a medium that participates in directly or indirectly providing signals, instructions and/or data. A computer-readable medium may take the forms, including but limited to, non-volatile medium, volatile media, and transmission media. Non-volatile media may include, for example, optical or magnetic disks, dynamic memory and the like. Transmission media may include coaxial cables, copper wire, fiber optic cables, and the like. Transmission media can also take the form of electromagnetic radiation, like that generated during radio-wave and infra-red data communications, or take the form of one or more groups of signals. Common forms of computer-readable medium include, but are not limited to, a floppy disk, a flexible disk, a hard disk, a magnetic tape, other magnetic medium, a CD-ROM, other optical medium, punch cards, paper tape, other physical medium with patterns and holes, a RAM, a ROM, an EPROM, a FLASH-EPROM, or other memory chip or card, a memory stick, a carrier wave/pulse, and other media from which a computer, a processor or other electronic device can read. Signals used to propagate instructions or other software over a network, like the Internet, can be considered a "computer-readable medium.

(Claim 22 and 24), are rejected under 35 U.S.C. 101 because the claims are not limited to tangible embodiments. In view of Applicant's discloser, specification (Page 3, Lines 9-24), the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., "Common forms of computer-readable medium include, but are not limited to, a floppy disk, a flexible disk, a hard disk, a magnetic tape..." (Page 3, Line 16-20)) and intangible

embodiments (e.g., "carrier wave/pulse" (Page 3, Line 19)). As such, the claims are not limited to statutory subject matter and are therefore non-statutory.

To vacate this rejection the claims and written description need to be amended to include only the physical computer storage medium and not a communication/transmission medium or other intangible or non-functional media.

The Examiner recommends the following changes to the written description:

> "Computer-readable storage medium", as used herein, refers to a medium that participates in directly or indirectly providing ~~signals~~ instructions and/or data. A computer-readable storage medium may take the forms, including but limited to, non-volatile medium, and volatile medium ~~media, and transmission media~~. Non-volatile medium ~~media~~ may include, for example, optical or magnetic disks, dynamic memory and the like. ~~Transmission media may include coaxial cables, copper wire, fiber optic cables, and the like. Transmission media can also take the form of electromagnetic radiation, like that generated during radio-wave and infra-red data communications, or take the form of one or more groups of signals.~~ Common forms of computer-readable storage medium include, but are not limited to, a floppy disk, a flexible disk, a hard disk, a magnetic tape, other magnetic medium, a CD-ROM, other optical medium, punch cards, paper tape, other physical medium with patterns and holes, a RAM, a ROM, an EPROM, a FLASH-EPROM, or other memory chip or card, a memory stick, ~~a carrier wave/pulse,~~ and other medium ~~media~~ from which a computer, a processor or other electronic device can read stored instructions and/or data from. ~~Signals used to propagate instructions or other software over a network, like the Internet, can be considered a "computer-readable medium.~~

"Signals" as used herein, refers to transmission media that may include coaxial cables, copper wire, fiber optic cables, and the like. Transmission media can also take the form of electromagnetic radiation, like that generated during radio-wave and infra-red data communications, or take the form of one or more groups of signals.

Please see attachment for clean copy of suggested replacement.

***Claim Rejections - 35 USC § 102***

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Bhatia et al. (US 6,535,798 B1 March 18, 2003).

Examiner Note: The Examiner will be evaluating the preceding claims in respect to functionality and processes and not by specific boundaries or components. It is ordinary in the art that multiple elements can be functionally separated and contained within multiple elements or contained within a single element or combinations thereof. Examiner refers to Applicant's written description "One of ordinary skill in the art will appreciate that one element may be designed as multiple elements or that multiple elements may be designed as one element. An element shown as an internal component of another element may be implemented as an external component and vice versa. Furthermore, elements may not be drawn to scale" (Page 2, Line 3) and in respect thereto the Examiner will evaluate the prior art.

Examiner Note: The Examiner will be evaluating the following terms in the following way:

a. **GPIO (General Purpose Input Output):** Any functional I/O (Input Output) processor, co-processor, register, computer-readable medium, and/or secondary chip that majority function is I/O routing, multiplexing, and/or switching (e.g. super I/O, bridge chip, I/O circuit, bus chip, router, etc).

b. **Register:** A register as a common term in the art is a storage area for the holding of data for a computer processor the storage area can be but not limited to a latch bank, I/O mapped memory, general memory, and/or system memory. The size of a register is determined by the type of processor, an 8-bit processor will have registers of minimum 8-bits in length, while a 32-bit processors registers are 32-bits in length and so on for 64 and 128-bit processors. At the time of filling March 2004 the general state of the art included 8-bit, 32-bit, and 64 bit processors.

c. **Set of Bits:** It is the Examiners evaluation that a single bit register can contain a bit from a set of bits in respect to the set being [0,1] and a single bit register selecting from the set [0,1] a sub-set of those bits being [0] or [1].

d. **Address:** It is the Examiners evaluation that an address in computer science is a set of bits that describes a specific location within memory (main and/or secondary) that contains data. An address when applicable to computer architecture can define a specific location within memory but can also define a specific architecture component such as a specific I/O port or system bus. The Examiner will evaluate an "address" in the broadest terms to include both computer architecture and computer science meanings.

e. **Frequency:** It is the Examiners evaluation of both throttling of a clock (stop/start) and increasing and/or decreasing the clock speed are equivalent in terms of the definition for frequency. Frequency as defined as the measurement of the number of times that a repeated event occurs per unit time meaning that throttling and clock speed increasing and/or decreasing are equivalent when evaluated over a period of time. Example: Clock running at 100 cycles per-second (100 Hz) (number of changes/time = frequency) now if the clock runs for only 0.5 seconds and is turn off for 0.5 seconds results in a frequency

of only 50 Hz resulting in a frequency change. The 50 Hz frequency can also be achieved by increasing the clock cycle by a factor of 2 resulting in a slower clock that would also decease the frequency to 50 Hz.

As per claims 1 and 22-23, Bhatia et al. discloses, "A system **[COMPUTER SYSTEM (Figure 1, 10)]** for simulating a processor performance state in a processor **["performance states (e.g., cycles the processor between a high and a low performance state)" (ABSTRACT)]**, comprising: a data structure stored in a memory, **[*software and/or applications are compilations of data structures including instructions stored in memory* (Column 5, Line 3-7)** and **"one or more ACPI objects" (Column 12, Line 46)** ***The "ACPI object" is a data structure.*]** the data structure being configured to store an address of a GPIO (general purpose input output) block **[*instructions associated with software and/or applications include instructions for the loading/storing of information in the storage medium and as a result the instructions contain relative/absolute memory addresses or memory address pointers* (Column 5, Line 9-11)** ***the addresses can indicate a location on the* "HOST BRIDGE" (Figure 1, 18)** ***or* "SYSTEM BRIDGE" (Figure 1, 34)** ***for the loading/storing of data.* "The location and structure of the control register may be defined under the ACPI object" (Column 12, Line 51)** and **"The control register may be defined in memory or I/O address space (Column 12, 43)** ***The examiner is equating I/O address space to a GPIO address*]** and a set of bit patterns **[*the ACPI specification which is incorporated by reference includes multiple defined states (e.g. set[ C1, C2, C3])* (Column 11, 20-23)** and **"ACPI object may define the number of performance states available" (Column 12, Line 53-57)** ***The ACPI object has been interpreted to contain multiple entries, equating to a set of entries one entry for each performance state and each performance state would be a specific bit pattern.*]** that may be written to one or more of, the GPIO block and a thermal management register in the processor, **[*the ACPI states are defined by loading the appropriate bit sequence into a thermal management register and reading from those register the***

***predefined values*** **(Column 7, Line 14-17) (Column 11, Line 8-10)** and **"writing a predefined value to a control register to indicate the new performance state of the processor (Column 12, Line 41)]** where the GPIO block is configured to control a thermal management signal that can be provided to the processor, **[*by changing the value loaded in the register the control signals associated with that register will be changed effecting the processor (i.e.* "In the illustrated embodiment, a signal G_LO/HI# from the system bridge 34, indicates the desired system state and controls the states of LO/HI# and VR_LO/HI#." (Column 11, Line 34))]**

and a logic **["FIG. 7, power management control logic" (Column 10, Line 39-51)]** operably connected to the memory, **["HOST BRIDGE" (Figure 1, 18), "RAM" (Figure 1, 16)]** the logic configured to receive a request **["SENSOR" (Figure 1, 15)** and **"notification when a sensed temperature rises above a preset target temperature $T_t$ or falls below the target temperature $T_t$" (Column 3, Line 24-46)]** to establish a desired processor performance state in the processor, **["for controlling the core clock frequency and the supply voltage level of the processor" (Column 10, Line 42)]** to select a bit pattern, the bit pattern being selected from the set of bit patterns, **[*by selecting one of the ACPI activity states the system has selected one state from the set and loaded the appropriate bit set into the register* (Column 11, Line 20-24) (Column 9, Line 46) (Column 12, Line 24-30)]** and to write the bit pattern to the GPIO block or the thermal management register, **["writing a predefined value to a control register to indicate the new performance state of the processor" (Column 12, Line 40-45)]** where the bit pattern facilitates controlling a frequency and a voltage at which the processor will operate, thus simulating the desired processor performance state:" **["internal control registers in the processor 12 may be used to program the performance state of the processor." (Column 11, Line 8)]**.

As per claim 2, Bhatia et al. discloses, "where the data structure is further configured to store an address of an ACPI status register **["The control register may be defined in memory or I/O address space" (Column 12, Line 43)** and **"the location and structure of the control register may be defined under an ACPI object" (Column 12, Line 44-57)** ***the "ACPI object" is a data structure that defines the location of the "control register" and since the control register can be defined in memory or as an I/O address the location would be a memory address or an I/O address (GPIO)]*** from which a value related to a frequency and a voltage established in the processor can be read." **["ACPI objects may define the number of performance states available, the core clock frequencies and supply voltage levels to be used in the performance states" (Column 12, Line 49-57)]**.

As per claim 3, Bhatia et al. discloses, "where the memory is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling a processor function." as **["A non-volatile memory 32 for storing BIOS routines may be located on the bus 46" (Column 3, Line 59-64)** and **"power management module may be implemented as a software module, in system firmware (e.g., system BIOS ... ) ... The power management module determines (at 122) if a performance state change is required)" (Column 12, Line 29-35)]**.

As per claim 4, Bhatia et al. discloses, "where the data structure comprises an ACPI table **["ACPI object may define the number of performance states available" (Column 12, Line 53-57)** ***the ACPI object has been interpreted to consist of a table since the object would contain multiple entries, one entry for each performance state which equates to a table]*** stored in a memory that is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling a processor function." ***[The ACPI object is part of the power management module which can be*** **"a software module, in system firmware (e.g., system BIOS"** ***meaning that the ACPI object is a software data structure stored in system memory or stored directly in the BIOS memory. (Column 12, Line 26-57)*** *and* **"The power management**

**module determines (at 122) if a performance state change is required)" (Column 12, Line 29-35)]**.

Examiner Note: The Examiner additionally refers Applicant to the ACPI Specification that discloses the ACPI table as part of the specification **(1.6 ACPI Specification and the Structure Of ACPI, Advanced Configuration and Power Interface Specification)**. The Examiner also notes that the operating system is contained within the main and/or secondary memory and that the ACPI Specification also discloses communication between the BIOS and OS as part of the ACPI standard **(Figure 1-1 OSPM/ACPI Global System, (Advanced Configuration and Power Interface Specification)**.

As per claims 5, Bhatia et al. discloses, "where the data structure comprises an ACPI table **["ACPI object may define the number of performance states available" (Column 12, Line 53-57)** ***the ACPI object has been interpreted to consist of a table since the object would contain multiple entries, one entry for each performance state which equates to a table***] stored in a Basic Input Output System (BIOS) configured to facilitate controlling a processor function." as **[*The ACPI object is part of the power management module which can be* "a software module, in system firmware (e.g., system BIOS" (Column 12, Line 26-57)** ***meaning that the ACPI object is a software data structure stored directly in the BIOS memory.*** *and* **"The power management module determines (at 122) if a performance state change is required)" (Column 12, Line 29-35)]**.

Examiner Note: The ACPI Standard discloses the application of an "ACPI BIOS".

As per claims 6, Bhatia et al. discloses, "where the set of bit patterns facilitates simulating two processor performance states that correspond to a higher performance state and a lower performance state." as **["more than two performance states may be defined, including a**

**lower performance (LP) state and two higher performance states, referred to as the HP1 and HP2 states" (Column 9, Line 46-49)** and **"Programming the control register ... ACPI objects may define the number of performance states available" (Column 12, Line 44-57)** ***The programming of the control registers is interpreted as loading the "control register" with a specific set of bits correlating to one of the many performance states defined in the "ACPI object".***].

As per claim 7, Bhatia et al. discloses, "where the thermal management register comprises the TM2 register in a Pentium microprocessor." as **["internal control registers in the processor 12 may be used to program the performance state of the processor." (Column 11, Line 8-9)]**.

Examiner Note: See 35 U.S.C. 112 Rejections.

As per claim 8, Bhatia et al. discloses, "where the thermal management signal comprises a signal placed on the PROCHOT line available to a Pentium microprocessor." as **["LO/HI#" (Figure 7)]**.

Examiner Note: See 35 U.S.C. 112 Rejections.

As per claim 9, Bhatia et al. discloses, "the system being incorporated into a computer" as **["COMPUTER SYSTEM" (Figure 1, 10)]**.

As per claim 11, Bhatia et al. discloses, "A system for simulating a processor performance state in a processor **["A system according to an embodiment of the invention implements a thermal management scheme in which one or more system components are switched between different levels (two or more) of performance states in response to over-temperature conditions or other conditions" (Column 2, Line 24-28)]** that is configured to receive an actual thermal management signal **["One or more temperature senor units 15**

**monitor system temperature in one or more corresponding thermal zones" (Column 3, Line 33-40)]** from a thermal management circuit **["a thermal management controller " (Column 2, Line 29)]** and to selectively change the processor operating frequency based on the thermal actual management signal, **["The power management control logic 100, 102 provides control signals to the voltage regulator 52 to adjust its voltage levels and the to the processor 12 to adjust the processor's internal clock frequency." (Column 10, Line 66: Column 11, Line 1-2)]** the system comprising: a simulation logic configured to produce a simulated thermal management signal; **["ACPI Specification ... one or more ACPI objects may be indicated to the operating system that the computer is capable of transiting between or among different performance states" (Column 12, Line 45-51)]** and a combination logic configured to selectively provide to the processor one and only one of, the actual thermal management signal and the simulated thermal management signal." **["The power management module determines (at 122) if a performance state change is required in response to a received event, indicating a thermal event, power supply transition, docking/undocking, a user command, or other event has occurred." (Column 12, Line 38-57), (Column 7-8, Line 57-39)**, and **(Figure 3)]**.

Examiner Note: The Examiner has interpreted the prior art as disclosing a system that can both vary the frequency and voltage of the processor in response to the temperature measured by a temperature sensor and also issue a system interrupt if the temperature continues to exceed threshold limits. The temperature (actual thermal management signal) is provided to the thermal management controller (logic) for evaluation and processing (combination logic). When the actual thermal management signal temperature exceeds a threshold limit the thermal management controller implements changes to the frequency and voltage of the processor. These performance states are simulated thermal management signals based on the ACPI Specification and implemented by the thermal management controller to manage the temperature of the processor/system. The thermal management controller will continue to decrease the

performance states until the temperature drops below the threshold limit. If the processor fails to drop below the threshold temperature limit after the thermal management controller has implemented the lowest performance level (simulated thermal management signal) the thermal management controller will then issue the actual thermal management signal as a system/processor in the form of an interrupt. **(Column 6-12)**.

As per claim 12, see rejection to claim 1.

As per claim 13, see rejection to claim 7 and 35 U.S.C. 112 Rejections.

As per claim 14, please see rejection to claim 1. Claim 14 is broader in scope than claim 1 and as a result is rejected on the basis that claim 1 has been rejected.

As per claim 15, see rejection to claim 5.

As per claim 16, Bhatia et al. discloses, "where establishing the data structure includes writing a set of bit patterns to the ACPI table **["ACPI objects may define the number of performance states available" (Column 12, Line 53-57)** ***The number of performance states has been evaluated as equating to a number of bit patterns (one pattern for each performance state) and a grouping of a number of individual performance states correlates to a table of performance stats contained in the ACPI object".***] and writing the address of the GPIO block to the ACPI table" **["The location and structure of the control register may be defined under the ACPI object" (Column 12, Line 51)** and **"The control register may be defined in memory or I/O address space" (Column 12, Line 43)** ***When the "control register" is defined in memory the "ACPI object" will contain the memory address (location) for the "control register" so that the "power management module" can write/read the desired bit pattern to the correct memory location. If the "control register" is "I/O address space" (GPIO) then***

***the "ACPI object" will also contain the address so that the "power management module" can write/read the desired bit pattern to the correct "I/O address space" (GPIO).]***

As per claim 17, see rejection to claim 6.

As per claim 18, see rejection to claim 1.

As per claim 19, see rejection to claim 7 and 35 U.S.C. 112 Rejections.

As per claim 20, see rejection to claim 8 and 35 U.S.C. 112 Rejections.

As per claim 21, Bhatia et al. discloses, "acquiring an address of an ACPI status register configured to report a value related to the operating frequency and the operating voltage of the processor;" **[Detection of whether the processor 12 is in the HP or LP state may be accomplished by reading predefined registers in the processor 12 or in other components in the system, including the voltage regulator 52 or the system memory 16. (Column 7, Line 13-17)** and **"The location and structure of the control register may be defined under the ACPI object" (Column 12, Line 51)]** "reading the value from the ACPI status register; and selectively reporting a success or error condition based on the value. **["After the internal clock frequency and voltage settings have changed, predefined register bits in the processor 12 may be updated that is accessible by software to determine if the performance state change has been successfully made. The predefined register bits may be mapped to a memory or I/O address of the processor 12, the voltage regulator 52, or a combination of both. Alternatively, the predefined register bits may be found in system memory 16." (Column 15, Line 38-45)].**

As per claim 24, Bhatia et al. discloses, "A set of application programming interfaces embodied on a computer-readable medium for execution by a computer component in conjunction with simulating a processor performance state in a processor by controlling a thermal management signal, comprising: **["The power management module may be implemented as a software module, in system firmware (e.g., system BIOS or SMI handler), as part of the operating system, as a device driver, or as a combination of the above." (Column 12, Line 31)]** a first interface for communicating a bit pattern data; **["the power management module indicates (at 124) the new performance state of the processor is to transition to. This may be performed, for example, by writing a predefined value to a control register to indicate the new performance state of the processor" (Column 12, Line 41)** ***The predefined value is equated to a bit pattern associated with a specific performance state***] a second interface for communicating a GPIO block address data; **["HOST BRIDGE" (Figure 1, 18), "SYSTEM BUS" (Figure 1, 22), "SYSTEM BRIDGE" (Figure 1, 34)**, and **"SECONDARY BUS" (Figure 1, 46)** ***This functional blocks and/or logic blocks transfer data between the processor and non-processor components]*** and a third interface for communicating a state data, where the state data is related to a simulated processor performance state generated by applying the bit pattern data to a GPIO block identified by the GPIO block address data." **["After the internal clock frequency and voltage settings have changed, predefined register bits in the processor 12 may be updated that is accessible by software to determine if the performance state change has been successfully made. The predefined register bits may be mapped to a memory or I/O address of the processor 12, the voltage regulator 52, or a combination of both. Alternatively, the predefined register bits may be found in system memory 16." (Column 15, Line 38-45)].**

Examiner Note: The applicant has only claimed an interface for communicating data between the system components. The applicant has not claimed the ability or application of a user/human interface for interfacing with the system as noted in Applicant Response. Examiner additionally

cautions Applicant about the addition of new matter, and refers Applicant to the ACPI Specification and the Microsoft's Windows Operating System's power management GUI.

***Claim Amendments 35 USC § 103***

17. The 35 USC § 103 rejections to the claims per Office Action mailed 06 November 2006 have been withdrawn due to amendments and remarks filed 06 February 2007.

***Claim Rejections - 35 USC § 103***

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatia et al. (US 6,535,798 B1 March 18, 2003) and general knowledge in the art.

As per claim 10, it would have been obvious to apply the same system to a printer as applicable to a computer system. Both a computer system and a printer system use microprocessors for processing electrical signals that generate heat and additional electrical components (e.g., power supply, mechanical parts) that also generate heat. Both systems are susceptible to over-heating conditions as a result of the microprocessors and electrical systems being confined within a closed space and as a result both require thermal monitoring and control. Both systems additionally implement mechanical means for discharging excessive heat through the usage of fans and/or vents and also power management associated with on, sleep, and off states.

***Response to Arguments***

20. The Examiner has reevaluated the prior art based on Applicants amendments and remarks filed 06 February 2007 and changed the basis of rejection and has presented them in this new non-final Office action as new grounds for rejection.

***Conclusion***

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan R. Plante whose telephone number is (571) 272-9780. The examiner can normally be reached on Monday -- Friday 10:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 2, 2007
JRP

Jonathan R Plante
ART UNIT 2182

KIM HUYNH
SUPERVISORY PATENT EXAMINER
4/4/07